FICER Technology Co., Ltd.
明虹科技股份有限公司

2F, No.138, Daye Rd., Beitou Dist.,
Taipei City 112030, Taiwan
www.Ficer.com

SKU: 00T0S03

# 200G QSFP56 SR4 Transceiver
# Hot Pluggable, MPO / MTP, 850nm VCSEL, OM3 70M / OM4 100M, DSP Solution, OIF-CMIS Management & DDM, C-Temp

## Part Number: FQ56-S9-M85-X1D-DS2



## Overview

FQ56-S9-M85-X1D-DS2 is a parallel fiber optical transceiver module for 212.5Gbps data transmission applications at 850nm. It is ideally suited for datacom & storage area network (SAN/NAS) applications based on IEEE 802.3cd 200GBASE-SR4 and InfiniBand HDR standard. Designed for short range multi-lane data communication, the QSFP56 full-duplex optical module with MPO-12 APC receptacle integrates four independent transmitter and receiver channels each capable 53.125Gbps operation for an aggregate data rate of 212.5Gbps up to MMF OM3 70m / OM4 100m optical links.

## Applications

- 200GBASE-SR4 Ethernet @212.5G
- Breakout to 4 x 50GBASE-SR Ethernet
- InfiniBand HDR interconnect
- Data Centers Switch Interconnect
- Server and Storage Area Network Interconnect

## Features

- Compliant with IEEE802.3cd 200GBASE-SR4
- Compliant with SFF-8665 QSFP56 MSA
- Compliant with IEEE 802.3bs 200GAUI-4 Interface
- 4 independent full-duplex channels
- Signaling Rate PAM4 26.5625GBd per Lane
- DSP with built in quad Tx CDR and Rx CDR
- Hot Pluggable QSFP56 footprint
- 4CH 850nm VCSEL array transmitter & PIN receiver
- MPO-12 APC receptacle connector
- 2-wire interface for management and diagnostic monitor compliant with OIF-CMIS
- Single 3.3V power supply
- Link distance 70m over OM3 fiber and 100m over OM4 fiber with KP4 FEC
- Operating Temperature 0~+70°C
- Maximum power consumption 4.5W
- RoHS compliant



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Link Fiber to Future
V3.50_20260923

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## Laser Safety

- This is a Class 1 Laser Product complies with 21 CFR 1040.10 and 1040.11 except for conformance with IEC 60825-1 Ed. 3., as described in Laser Notice No. 56, dated May 8, 2019.
- Caution: Use of control or adjustments or performance of procedure other than those specified herein may result in hazardous radiation exposure.

## Absolute Maximum Ratings

| Parameters | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| Storage Temperature | $T_{ST}$ | -40 | +85 | °C |
| Relative Humidity | RH | 5 | 85 | % |
| Supply Voltage | $V_{CC}$ | -0.5 | +3.6 | V |

## Recommended Operating Conditions

| Parameters | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Case Operating Temperature | $T_{OP}$ | 0 | - | +70 | °C |
| Supply Voltage | $V_{CC}$ | +3.13 | +3.3 | +3.47 | V |
| Electrical Signaling Rate, per Lane (PAM4) | | | 26.5625 | | GBd |
| Optical Signaling Rate, per Lane (PAM4) | | | 26.5625 | | GBd |
| Data Rate Accuracy | ΔDR | -100 | | +100 | ppm |
| Bit Error Rate (Pre-FEC) | BER | | | $2.4x10^{-4}$ | |
| Bit Error Rate (Post-FEC) | $I_{CC}$ | | | $1x10^{-12}$ | |
| Supply Current (+3.3V) | P | | | 1360 | mA |
| Power Consumption | | | | 4.5 | W |
| Transceiver Power-on Initialization Time | $V_{IH}$ | | | 2000 | ms |



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## Transmitter Electro-optical Characteristics

**$V_{CC}$ = 3.13V to 3.47V, $T_{OP}$ = 0 °C to +70 °C**

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Optical Signaling Rate, per Lane | | | 26.5625 | | GBd | PAM4 |
| Optical Wavelength, each Lane | λc | 840 | 850 | 860 | nm | |
| Spectral Width (RMS) (Modulated) | Δλ | | | 0.6 | nm | |
| Average Launch Power, per Lane | $P_{AVG}$ | -6.5 | | +4 | dBm | 1 |
| Outer Optical Modulation Amplitude ($OMA_{Outer}$), per Lane | $P_{OMA}$ | -4.5 | | +3 | dBm | 2 |
| Launch Power in $OMA_{Outer}$ minus TDECQ, per Lane | OMA-TDECQ | -5.9 | | | dB | |
| Transmitter and Dispersion Eye Clouser for PAM4, per Lane | TEQCQ | | | 4.5 | dB | 3 |
| Optical Extinction Ratio | ER | 3 | | | dB | |
| Average Launch Power OFF, per Lane | $P_{OFF}$ | | | -30 | dBm | |
| Optical Return Loss Tolerance | ORLT | | | 12 | dB | |
| Input Differential Impedance | $Z_{IN}$ | 90 | 100 | 110 | Ω | |
| Differential Data Input Voltage | $V_{IN-PP}$ | 300 | | 900 | mVpp | |
| Differential Termination Mismatch | | | | 10 | % | |
| Single-ended Voltage Tolerance Range | | -0.4 | | 3.3 | V | |
| DC Common Mode Input Voltage | $CMV_{IN}$ | -350 | | 2850 | mV | 4 |

**Note1:** Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

**Note2:** Even if the TDECQ < 1dB, the $OMA_{Outer}$ (min) must exceed the minimum value specified here.

**Note3:** TDECQ is specified and measured as per IEEE802.3.cm Clause 150.8.5.

**Note4:** DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

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## Receiver Electro-optical Characteristics

**$V_{CC}$ = 3.13V to 3.47V, $T_{OP}$ = 0 °C to +70 °C**

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Optical Signaling Rate, per Lane | $DR_{OP}$ | | 26.5625 | | GBd | PAM4 |
| Optical Wavelength, each Lane | λc | 840 | 850 | 860 | nm | |
| Damage Threshold, per Lane | $D_{TH}$ | +5 | | | dBm | 1 |
| Average Receive Power, per Lane | $P_{RX-AVG}$ | -8.4 | | +4 | dBm | 2 |
| Receive Power ($OMA_{Outer}$), per Lane | $P_{RX-OMA}$ | | | +3 | dBm | |
| Receive Sensitivity ($OMA_{Outer}$), per Lane | $SEN_{OMA}$ | Max (-6.5, SECQ-7.9) | | | dBm | 3 |
| Stressed Receiver Sensitivity ($OMA_{Outer}$), per Lane | $SRS_{OMA}$ | | | -3.4 | dBm | 4 |
| Receiver Reflectance | $R_{RX}$ | | | -12 | dB | |
| LOS De-Assert | $LOS_D$ | | | -12 | dBm | |
| LOS Assert | $LOS_A$ | -30 | | | dBm | |
| LOS Hysteresis | $LOS_{HY}$ | 0.5 | | | dB | |
| Output Differential Impedance | $Z_{OUT}$ | 90 | 100 | 110 | Ω | |
| Differential Data Output Voltage | $V_{OUT-PP}$ | 300 | | 900 | mVpp | |
| Near-end Eye Symmetry Mask Width (ESMW) | | 0.265 | | | UI | |
| Near-end Eye Height, Differential | | 70 | | | mV | |
| Far-end Eye Symmetry Mask Width (ESMW) | | 0.2 | | | UI | |
| Far end Eye Height, Differential | | 30 | | | mV | |
| Transition Time, 20% to 80% | | 9.5 | | | ps | |
| DC Common Mode Output Voltage | $CMV_{OUT}$ | -350 | | 2850 | mV | 5 |

**Note1:** The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.

**Note2:** Average receive power, per lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

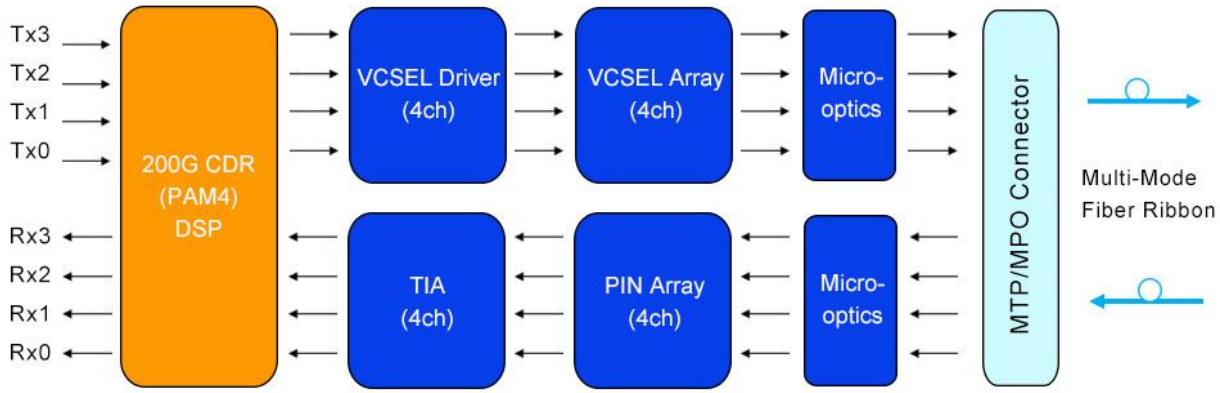
**Note3:** Receiver sensitivity is informative and is defined for a transmitter with a value of SECQ up to 4.5dB.

**Note4:** Measured with conformance test signal at receiver input for the BER of $2.4 \times 10^{-4}$.

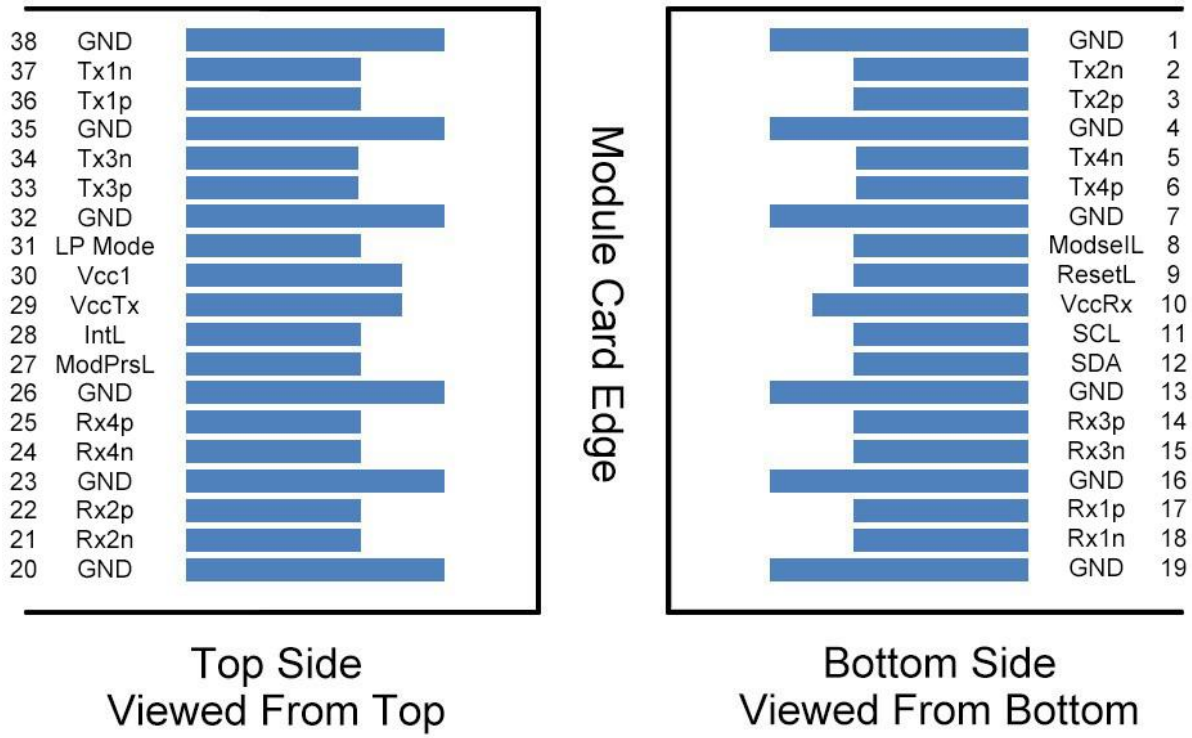
**Note5:** DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

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## Transceiver Block Diagram




## Pin Assignment




Top Side
Viewed From Top

Bottom Side
Viewed From Bottom

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## Pin Description

| Pin | Logic | Name | Function / Description |
|---|---|---|---|
| 1 | | GND | Module Ground |
| 2 | CML-I | Tx2n | Transmitter Inverted Data Input |
| 3 | CML-I | Tx2p | Transmitter Non-Inverted Data Input |
| 4 | | GND | Module Ground |
| 5 | CML-I | Tx4n | Transmitter Inverted Data Input |
| 6 | CML-I | Tx4p | Transmitter Non-Inverted Data Input |
| 7 | | GND | Module Ground |
| 8 | LVTLL-I | ModSelL | Module Select |
| 9 | LVTLL-I | ResetL | Module Reset |
| 10 | | VccRx | +3.3V Power Supply Receiver |
| 11 | LVCMOS-I/O | SCL | 2-Wire Serial Interface Clock |
| 12 | LVCMOS-I/O | SDA | 2-Wire Serial Interface Data |
| 13 | | GND | Module Ground |
| 14 | CML-O | Rx3p | Receiver Non-Inverted Data Output |
| 15 | CML-O | Rx3n | Receiver Inverted Data Output |
| 16 | | GND | Module Ground |
| 17 | CML-O | Rx1p | Receiver Non-Inverted Data Output |
| 18 | CML-O | Rx1n | Receiver Inverted Data Output |
| 19 | | GND | Module Ground |
| 20 | | GND | Module Ground |
| 21 | CML-O | Rx2n | Receiver Inverted Data Output |
| 22 | CML-O | Rx2p | Receiver Non-Inverted Data Output |
| 23 | | GND | Module Ground |
| 24 | CML-O | Rx4n | Receiver Inverted Data Output |
| 25 | CML-O | Rx4p | Receiver Non-Inverted Data Output |
| 26 | | GND | Module Ground |
| 27 | LVTLL-O | ModPrsL | Module Present |
| 28 | LVTLL-O | IntL | Interrupt |
| 29 | | VccTx | +3.3V Power Supply Transmitter |
| 30 | | Vcc1 | +3.3V Power Supply |
| 31 | LVTLL-I | LPMode | Low Power Mode |
| 32 | | GND | Module Ground |



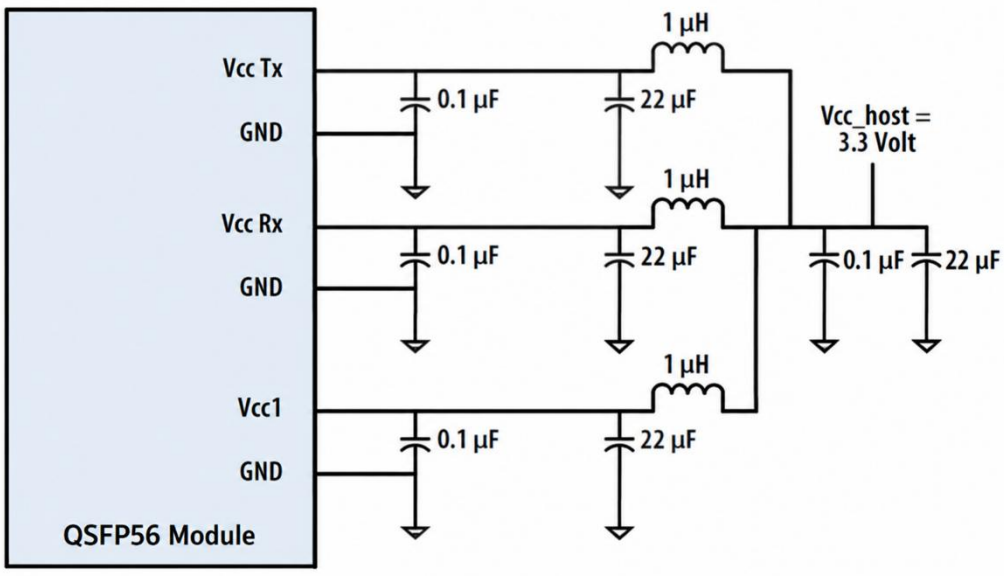
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| | | | |
|---|---|---|---|
| 33 | CML-I | Tx3p | Transmitter Non-Inverted Data Input |
| 34 | CML-I | Tx3n | Transmitter Inverted Data Input |
| 35 | | GND | Module Ground |
| 36 | CML-I | Tx1p | Transmitter Non-Inverted Data Input |
| 37 | CML-I | Tx1n | Transmitter Inverted Data Input |
| 38 | | GND | Module Ground |

**Note1:** GND is the symbol for signal and supply (power) common for QSFP56 modules. All are common within the QSFP56 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground lane.

**Note2:** VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP56 transceiver module in any combination. The connector pins are each rated for a maximum current of 1000mA.

## Recommended Power Supply Filter



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## Digital Diagnostic Functions

As defined by the QSFP56 MSA, Ficer's QSFP56 transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

- Transceiver temperature
- Laser bias current (4-Channel)
- Transmitted optical power (4-Channel)
- Received optical power (4-Channel)
- Transceiver supply voltage

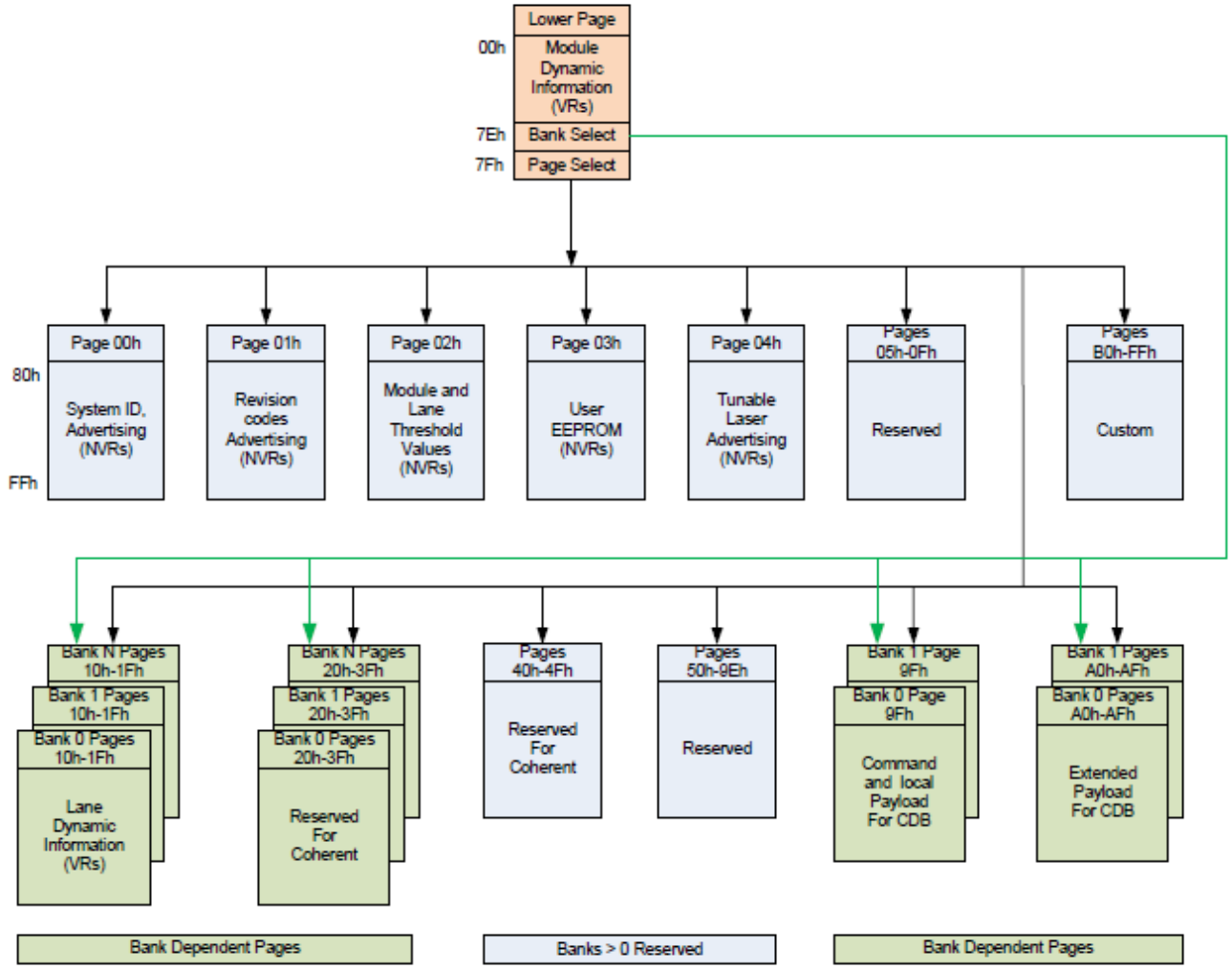
It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Controller (DDC) inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the QSFP56 transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the QSFP56 transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 000h to the maximum address of the memory.

For more detailed information including memory map definitions, please see the QSFP56 MSA Specification.

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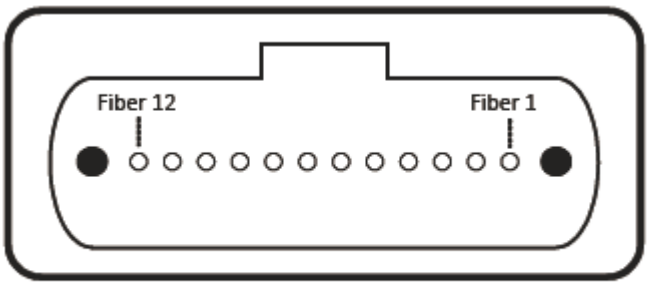
## Digital Diagnostic Memory Map (CMIS)



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Taipei City 112030, Taiwan
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## Optical Interface Lanes and Assignment




Outside View of the QSFP56 Module MPO-12

| Fiber # | Lane Assignment |
|---|---|
| 1 | Rx0 |
| 2 | Rx1 |
| 3 | Rx2 |
| 4 | Rx3 |
| 5,6,7,8 | Not used |
| 9 | Tx3 |
| 10 | Tx2 |
| 11 | Tx1 |
| 12 | Tx0 |

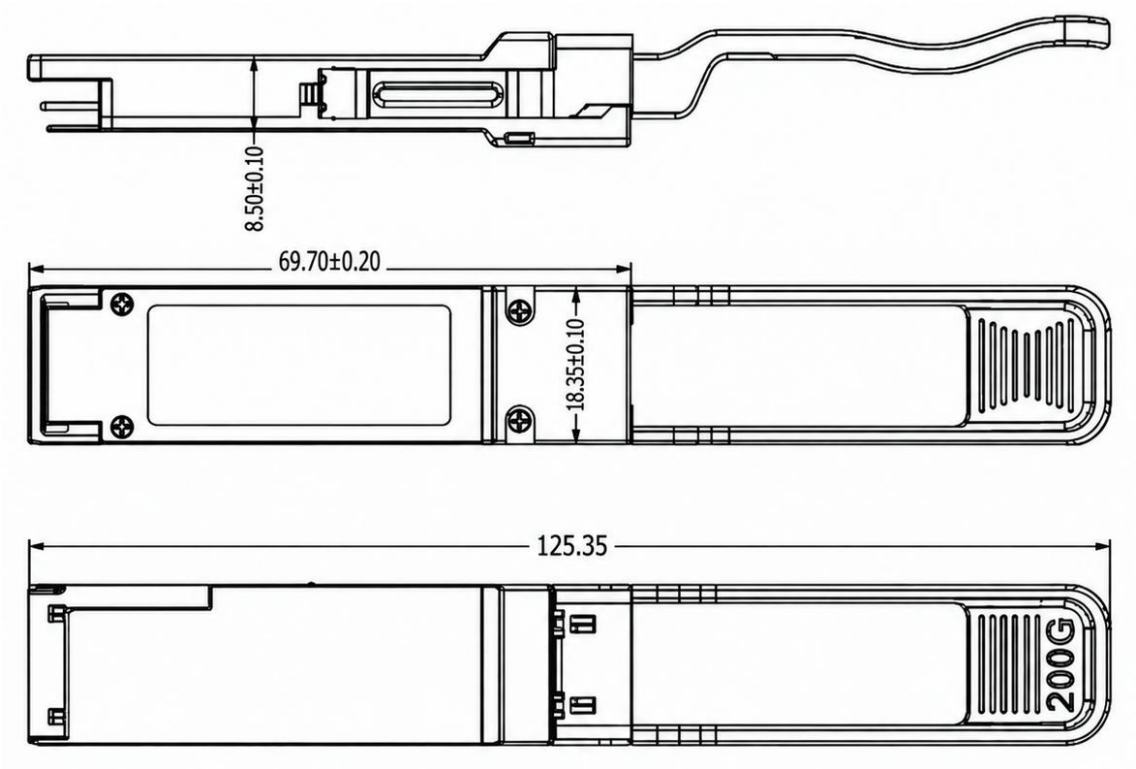
lane assignment



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## Mechanical Dimensions




**(All Dimensions are ±0.20mm Unless Otherwise Specified, Unit: mm)**

## Ordering Information

| Part No. | Tx | Rx | Link | DDM | Temp. |
|---|---|---|---|---|---|
| FQ56-S9-M85-X1D-DS2 | 850 nm | 850 nm | MM OM3 70m<br>MM OM4 100m | Yes | 0~+70°C |

**Note:** Distances are indicative only. To calculate a more precise link budget based on specific conditions in your application, please refer to the optical characteristics.



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