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SKU: 04C0T01

400G QSFP112 SR4 Transceiver
Hot Pluggable, MPO / MTP-12, 850nm VCSEL, OM3 60M / OM4 100M
CMIS Management & DDM, C-Temp

Part Number: FQA2-T9-M85-X1D



Overview

FQA2-T9-M85-X1D is a parallel fiber QSFP112 optical transceiver with MPO-12 connector for short-reach 400G data communication and interconnect applications using multi-mode fiber. The transceiver receives 4x100Gb/s (PAM4) Host electrical input data and converts that to 4x100Gb/s (PAM4) parallel optical signals. Reversely, on the receiver side, it converts 4x100Gb/s parallel optical signals into 4x100Gb/s electrical output data. It achieves an aggregated data rate of 400Gb/s up to MMF OM4 100m optical link with Host FEC.

Applications

- 400GBASE-SR4 Ethernet @425G
- Data Centers Switch Interconnect
- Server and Storage Area Network Interconnect

Features

- Compliant with IEEE 802.db 400GBASE-SR4
- Compliant with QSFP112 MSA V2.0
- Compliant with IEEE 802.3ck 400GAUI-4 Interface
- 4 Parallel full-duplex Lanes
- Optical Data Rate PAM4 53.125GBd per Lane
- Electrical Data Rate PAM4 53.125GBd per Lane
- Support aggregated data rate up to 425Gb/s
- Built in quad Tx CDR and Rx CDR
- Support KP4 FEC at 400Gbps
- Hot Pluggable QSFP112 footprint
- MPO-12 APC connector
- 2-wire interface for management and diagnostic monitor compliant with OIF-CMIS
- Single 3.3V power supply
- Link distance 100m over OM4 fiber and 60m over MM OM3 fiber
- Operating Temperature 0~+70°C
- Maximum power consumption 8W
- RoHS compliant

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Laser Safety

- This is a Class 1 Laser Product complies with 21 CFR 1040.10 and 1040.11 except for conformance with IEC 60825-1 Ed. 3., as described in Laser Notice No. 56, dated May 8, 2019.
- Caution: Use of control or adjustments or performance of procedure other than those specified herein may result in hazardous radiation exposure.

Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit
Storage Temperature	T_{ST}	-40	+85	°C
Storage Relative Humidity	RH	0	85	%
Supply Voltage	V_{CC}	-0.5	+3.6	V

Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Unit
Case Operating Temperature	T_{OP}	0	-	+70	°C
Supply Voltage	V_{CC}	+3.13	+3.3	+3.47	V
Data Rate, per Lane (PAM4)	DR		53.125		GBd
Data Rate Accuracy	ΔDR	-100		+100	ppm
Bit Error Rate (Pre-FEC)	BER			$2.4x10^{-4}$	
Bit Error Rate (Post-FEC)	BER			$1x10^{-12}$	
Supply Current	I_{CC}			2400	mA
Power Consumption (+3.3V)	P			8	W
Transceiver MgmtInit Duration				2000	ms
Control Input Voltage High	V_{IH}	2.0		Vcc+0.3	V
Control Input Voltage Low	V_{IL}	-0.3		0.8	V
Control Output Voltage High	V_{OH}	Vcc-0.5		Vcc+0.3	V
Control Output Voltage Low	V_{OL}	GND		0.4	V

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Transmitter Electro-optical Characteristics

V_{CC} = 3.13V to 3.47V, T_{OP} = 0 °C to 70 °C

Parameters		Symbol	Min.	Typ.	Max.	Unit	Note
Optical Data Rate, per Lane		DR_{OP}		53.125		GBd	PAM4
Optical Wavelength, λ		λ_1	844	850	863	nm	
Spectral Width (RMS) (Modulated)		Δλ			0.6	nm	
Average Launch Power, per Lane		P_{AVG}	-4.6		+4	dBm	1
Outer Optical Modulation Amplitude (OMA_{Outer}), per Lane X= MAX(TECQ, TDECQ)	X ≦ 1.8dB	P_{OMA}	-2.6		+3.5	dBm	2
	1.8 < X ≦4.4dB.		-4.4+X		+6.4	dBm	
Transmitter and Dispersion Eye Clouser for PAM4(TDECQ), per Lane		TDECQ			4.4	dB	3
Transmitter Eye Clouser for PAM4, per Lane		TECQ			4.4	dB	
Optical Extinction Ratio		ER	2.5			dB	
RIN12 OMA		RIN_{OMA}			-132	dB/Hz	
Average Launch Power OFF, per Lane		P_{OFF}			-30	dBm	
Optical Return Loss Tolerance		ORLT			14	dB	
Encircled Flux			≧86% at 19um ≦30% at 4.5um				4
Electrical Data Rate, per Lane (TP1)		DR_{EL}		53.125		GBd	PAM4
Differential Data Input Voltage (TP1a)		V_{IN-PP}	900			mVpp	5
Differential Termination Mismatch (TP1)					10	%	
Single-ended Voltage Tolerance Range (Min) (TP1a)			-0.4		3.3	V	
DC Common Mode Input Voltage (TP1)		CMV_{IN}	-350		2850	mV	6

Note1: Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

Note2: Even if the TDECQ < 1.4 dB, the OMA_{Outer} (min) must exceed this value.

Note3: TDECQ is specified and measured as per IEEE802.3.cm Clause 150.8.5.

Note4: If measured into type A1a.2, or type A1a.3, or type A1a.4, 50 um fibers in accordance with IEC 61280-1-4.

Note5: With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.

Note6: DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

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Receiver Electro-optical Characteristics

V_{CC} = 3.13V to 3.47V, T_{OP} = 0 °C to 70 °C

Parameters		Symbol	Min.	Typ.	Max.	Unit	Note
Optical Data Rate, per Lane (PAM4)		DR_{OP}		53.125		GBd	PAM4
Optical Wavelength		λ_1	842		948	nm	
Damage Threshold, per Lane		D_{TH}	+5				1
Average Receive Power, per Lane		P_{RX-AVG}	-6.4		+4	dBm	2
Receive Power (OMA_{Outer}), per Lane		P_{RX-OMA}			+3.5	dBm	
Receiver Sensitivity (OMA_{Outer}), per Lane	TECQ≦ 1.8dB	SEN_{OMA}	-4.6			dBm	3
	1.8 < TECQ ≦4.4dB.		-6.4+TECQ				
Stressed Receiver Sensitivity (OMA_{Outer}), per Lane		SRS_{OMA}			-2		4
Receiver Reflectance		R_{RX}			-15	dB	
LOS De-Assert		LOS_D			-8.9	dBm	
LOS Assert		LOS_A	-15			dBm	
LOS Hysteresis		LOS_{HY}	0.5	1.5		dB	
Electrical Data Rate, per Lane		DR_{EL}		53.125		GBd	PAM4
Differential Data Output Voltage (TP4)		V_{OUT-PP}			900	mVpp	
AC Common Mode Output Voltage, RMS (TP4)					17.5	mV	
Differential Termination Mismatch (TP4)					10	%	
Transition Time, 20% to 80% (TP4)			8.5			ps	
Near-end Eye Height, Differential (TP4)			24			mV	
Near-end vertical eye closure (TP4)					7.5	dB	
Far end Eye Height, Differential (TP4)			24			mV	
Far-end vertical eye closure (TP4)					7.5	dB	
Effective return loss, ERL (TP4)			8.5			dB	
DC Common Mode Output Voltage (TP4)		CMV_{OUT}	-350		2850	mV	5
Conditions of Stress Receiver Sensitivity Test							
Stressed Eye Closure for PAM4 (SECQ), Lane under Test				4.4		dB	
OMA_{Outer} of each Aggressor Lane				3.5		dBm	

Note1: The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.

Note2: Average receive power, per lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

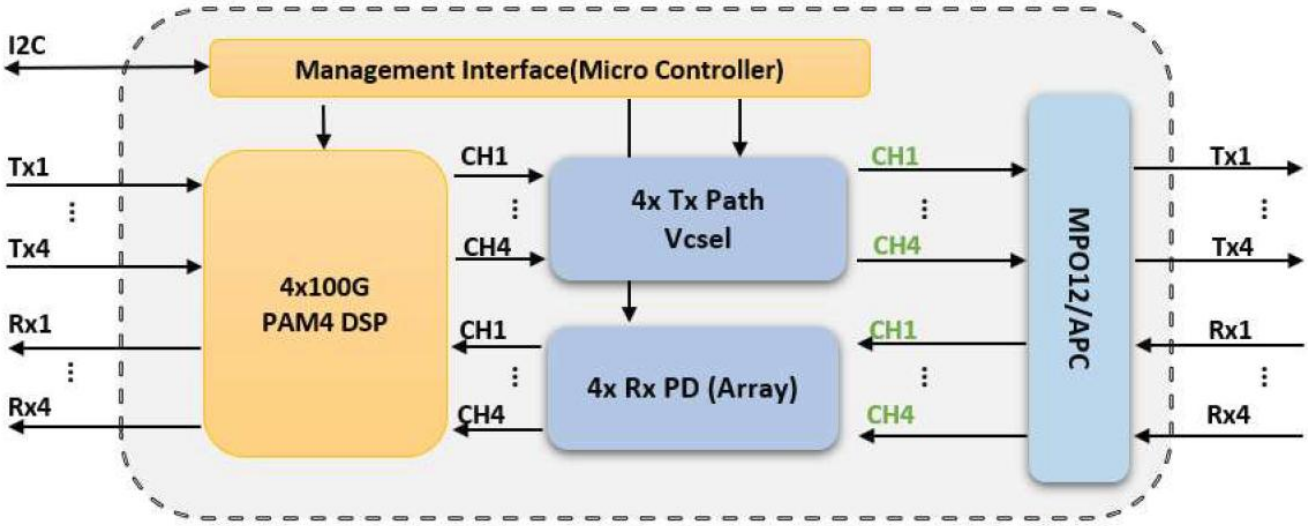
Note3: Receiver sensitivity is considered a normative requirement. RX sensitivity is defined for a transmitter with a value of SECQ up to 4.5dB.

Note4: Measured with a conformance test signal at TP3 (see IEEE 802.3 Cl 150) for the BER specified. They are not characteristics of the receiver. The conditions for measuring stressed receiver sensitivity are the following.

Stressed eye closure (SECQ), lane under test	4.5dB
SECQ – 10log10(Ceq) lane under test	4.5dBm
OMAouter of each aggressor lane	3.0dBm

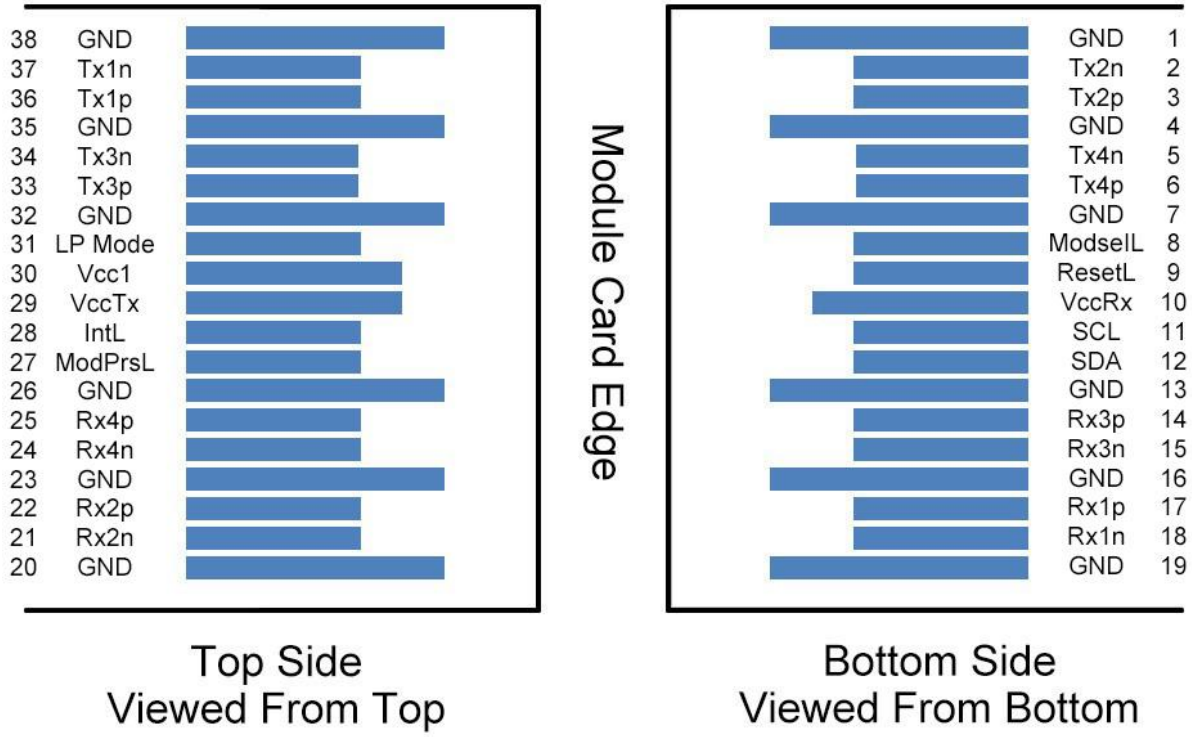
Note5: DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

Transceiver Block Diagram



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Pin Assignment



Pin Description

Pin	Logic	Name	Function / Description
1		GND	Module Ground
2	CML-I	Tx2n	Transmitter Inverted Data Input
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input
4		GND	Module Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7		GND	Module Ground
8	LVTLL-I	ModSelL	Module Select
9	LVTLL-I	ResetL	Module Reset
10		VccRx	+3.3V Power Supply Receiver
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data
13		GND	Module Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output

15	CML-O	Rx3n	Receiver Inverted Data Output
16		GND	Module Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19		GND	Module Ground
20		GND	Module Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-Inverted Data Output
23		GND	Module Ground
24	CML-O	Rx4n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-Inverted Data Output
26		GND	Module Ground
27	LVTLL-O	ModPrsL	Module Present
28	LVTLL-O	IntL	Interrupt
29		VccTx	+3.3V Power Supply Transmitter
30		Vcc1	+3.3V Power Supply
31	LVTLL-I	LPMode	Low Power Mode
32		GND	Module Ground
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input
34	CML-I	Tx3n	Transmitter Inverted Data Input
35		GND	Module Ground
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input
37	CML-I	Tx1n	Transmitter Inverted Data Input
38		GND	Module Ground

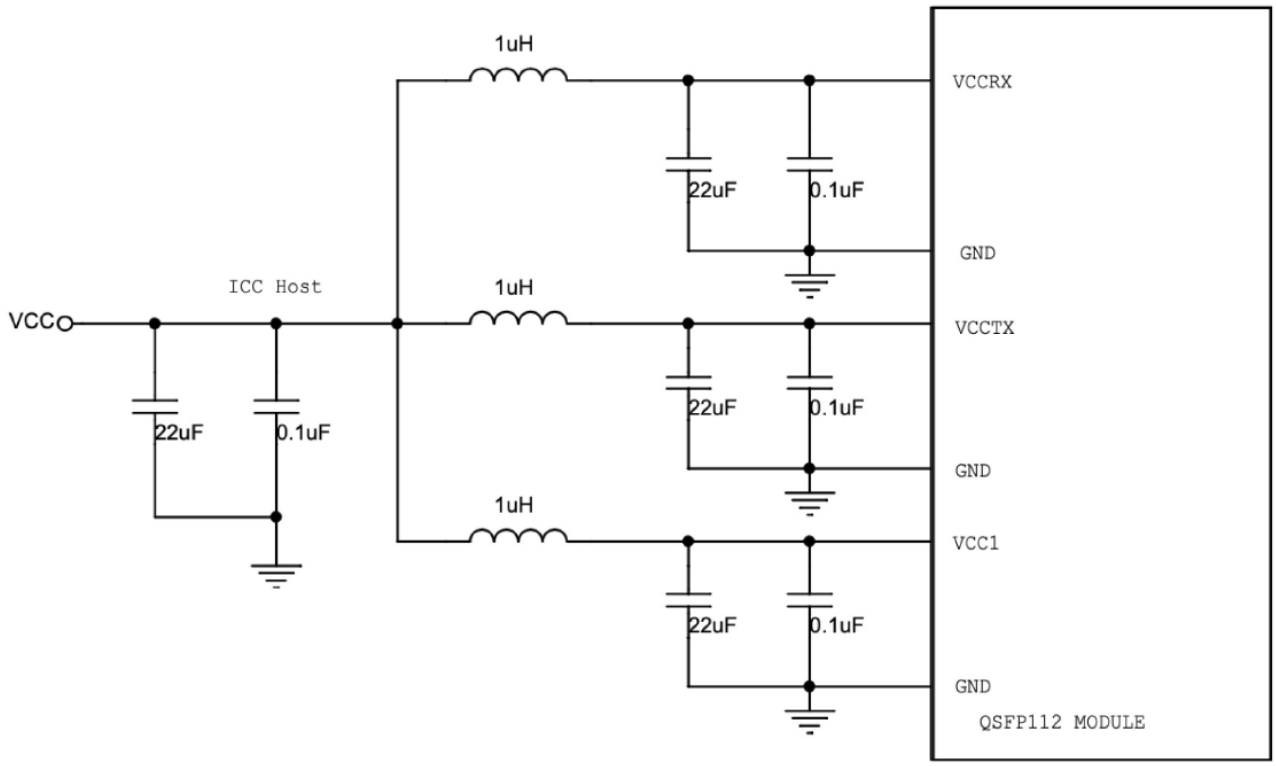
Note1: GND is the symbol for signal and supply (power) common for QSFP112 modules. All are common within the QSFP112 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground lane.

Note2: VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP112 transceiver module in any combination. The connector pins are each rated for a maximum current of 1500mA (2.0 A is required for high module power of 15-20W).

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Recommended Power Supply Filter



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Digital Diagnostic Functions

As defined by the QSFP112 MSA, Ficer's QSFP112 transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

- Transceiver temperature
- Laser bias current (4-Channel)
- Transmitted optical power (4-Channel)
- Received optical power (4-Channel)
- Transceiver supply voltage

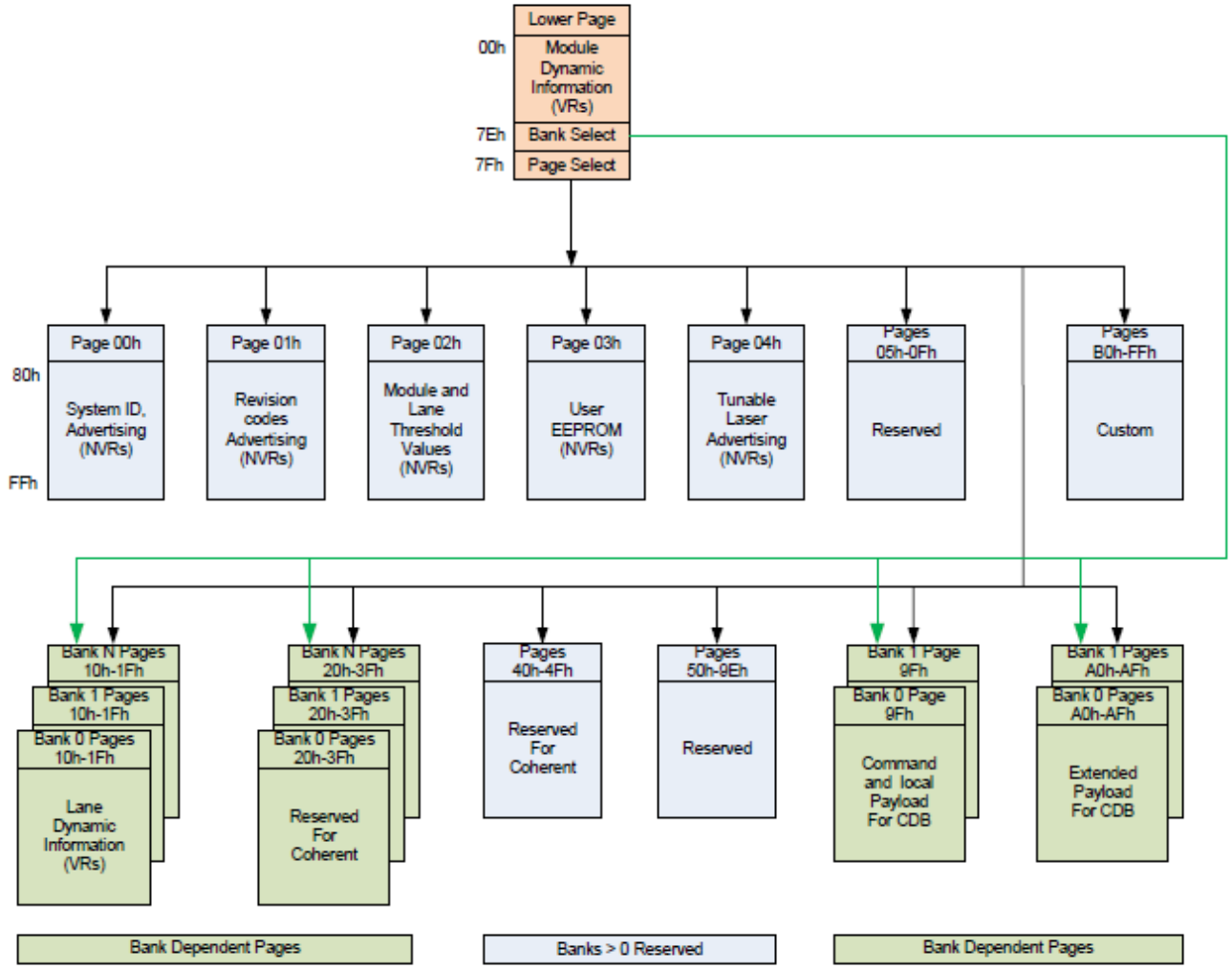
It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Controller (DDC) inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the QSFP112 transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the QSFP112 transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 000h to the maximum address of the memory.

For more detailed information including memory map definitions, please see the QSFP112 MSA Specification.

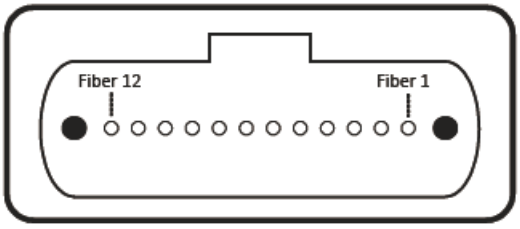
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Digital Diagnostic Memory Map (CMIS)



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Optical Interface Lanes and Assignment



Outside View of the QSFP28 Module MPO

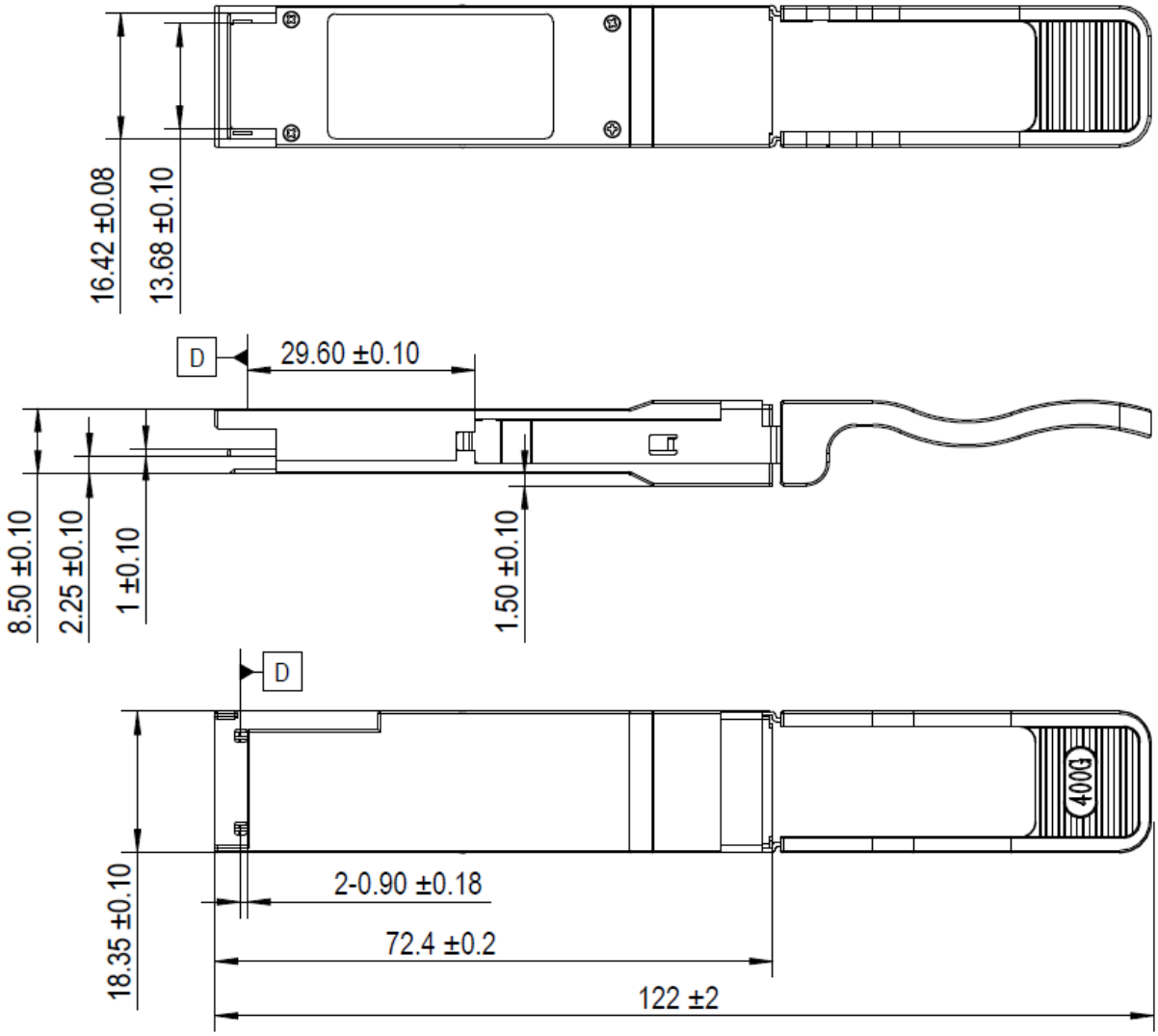
Fiber #	Lane Assignment
1	RX0
2	RX1
3	RX2
4	RX3
5,6,7,8	Not used
9	TX3
10	TX2
11	TX1
12	TX0

lane assignment

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Mechanical Dimensions



(All Dimensions are ±0.20mm Unless Otherwise Specified, Unit: mm)

Ordering Information

Part No.	Tx	Rx	Link	DDM	Temp.
FQA2-T9-M85-X1D	850nm	850nm	MM OM3 60m MM OM4 100m	Yes	0~70°C

Note: Distances are indicative only. To calculate a more precise link budget based on specific conditions in your application, please refer to the optical characteristics.