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Rev. 00U3.30_20230814

40G QSFP+ BiDi Receiver Only
Hot Pluggable, Dual BiDi LC, 850 / 908nm, MMF Rx SEN<-6.5dBm, DDM

Part Number: FQFP- IQ-C85-X1D

Overview

FQFP-IQ-C85-X1D is a pluggable optical receiver module with a Dual BiDi LC connector for 40G data monitoring applications using multi-mode fiber. It allows reuse existing MMF cabling infrastructure for easy migration to 40 Gigabit Ethernet connectivity. The receiver internally convert 2x20G optical channels into 2x20G electrical channels, then multiplexes that to XLPPI 4x10G interface channels, then for an aggregated receiving data rate of 40G up to sensitivity<-6.5dB on MMF.

Applications

- 40GBASE-SR2 Ethernet @41.3G
- 40Gbps Data Monitoring

Features

- Compatible with 40GBASE-SR2 BiDi
- Compliant with SFF-8436 QSFP+ MSA
- Compliant with IEEE 802.3ba-2010 40GbE XLPPI Interface
- Dual wavelength 850/908nm optical interface
- Up to 11.2Gbps data rate per 10G channel
- Built in quad Rx CDR
- Hot Pluggable
- Dual BiDi LC connector
- 2-wire interface for management and diagnostic monitor compliant with SFF-8436, SFF-8636
- Single 3.3V power supply
- Rx Sensitivity<-6.5dBm on MMF
- Maximum power consumption 3.5W
- RoHS compliant

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Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit
Storage Temperature	T_{ST}	-40	+85	°C
Storage Relative Humidity	RH	0	85	%
Supply Voltage	V_{CC3}	-0.5	+3.6	V

Recommended Operating Conditions

Parameters	Symbol	Min.	Typ.	Max.	Unit
Case Operating Temperature	T_{OP}	0	-	+70	°C
Supply Voltage	V_{CC}	+3.13	+3.3	+3.47	V
Electrical Data Rate, per Lane	DR_{EL}		10.3125	11.2	Gb/s
Data Rate Accuracy	ΔDR	-100		+100	ppm
Bit Error Rate (NO FEC)	BER			$5x10^{-5}$	
Supply Current	I_{CC}		750	1000	mA
Power Consumption	P		2.5	3.5	W
Transceiver Power-on Initialization Time				2000	ms
Control Input Voltage High	V_{IH}	2.0		Vcc	V
Control Input Voltage Low	V_{IL}	GND		0.7	V
Control Output Voltage High	V_{OH}	2.0		Vcc	V
Control Output Voltage Low	V_{OL}	GND		0.7	V

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Receiver Electro-optical Characteristics

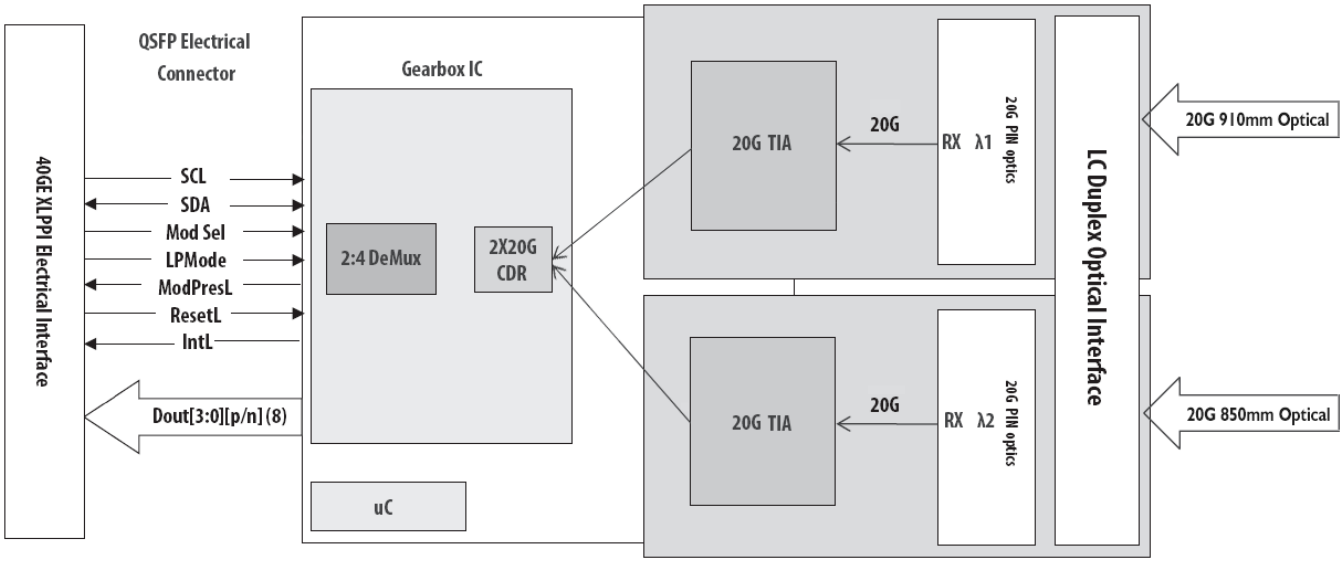
V_{CC} = 3.13V to 3.47V, T_{OP} = 0 °C to 70 °C

Parameters	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Data Rate, per Optical Channel	DR_{OP-R}		20.625		Gb/s	
Maximum Receive Power, per Channel	P_{RX-MAX}	+5			dBm	1
Receiver Sensitivity, per Channel	SEN			-6.5	dBm	2
Optical Wavelength, CH1	λ_{CH1}	882	908	918	nm	
Optical Wavelength, CH2	λ_{CH2}	832	850	868	nm	
Receiver Reflectance	R_{RX}			-12	dB	
LOS De-Assert	LOS_D			-8.6	dBm	
LOS Assert	LOS_A	-30	-14		dBm	
LOS Hysteresis	LOS_{HY}	0.5			dB	
Output Differential Impedance	Z_{OUT}	80	100	120	Ω	
Differential Data Output Voltage	V_{OUT-PP}	300	600	800	mVpp	

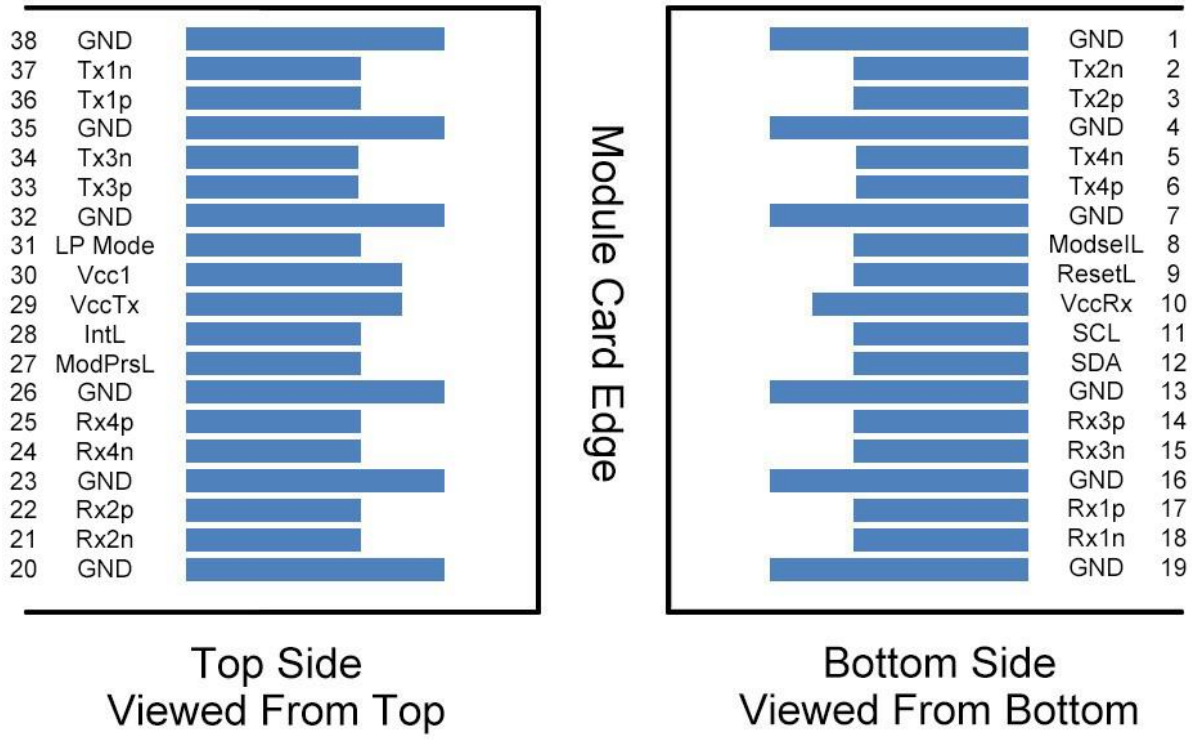
Note1: The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.

Note2: Measured with conformance test signal at receiver input for BER= $5x10^{-5}$.

Transceiver Block Diagram



Pin Assignment



Top Side
Viewed From Top

Bottom Side
Viewed From Bottom

Pin Description

Pin	Logic	Name	Function / Description
1		GND	Module Ground
2	CML-I	Tx2n	No Use
3	CML-I	Tx2p	No Use
4		GND	Module Ground
5	CML-I	Tx4n	Transmitter Inverted Data Input
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input
7		GND	Module Ground
8	LVTLL-I	ModSelL	Module Select
9	LVTLL-I	ResetL	Module Reset
10		VccRx	+3.3V Power Supply Receiver
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data
13		GND	Module Ground
14	CML-O	Rx3p	Receiver Non-Inverted Data Output
15	CML-O	Rx3n	Receiver Inverted Data Output
16		GND	Module Ground
17	CML-O	Rx1p	Receiver Non-Inverted Data Output
18	CML-O	Rx1n	Receiver Inverted Data Output
19		GND	Module Ground
20		GND	Module Ground
21	CML-O	Rx2n	Receiver Inverted Data Output
22	CML-O	Rx2p	Receiver Non-Inverted Data Output
23		GND	Module Ground
24	CML-O	Rx4n	Receiver Inverted Data Output
25	CML-O	Rx4p	Receiver Non-Inverted Data Output
26		GND	Module Ground
27	LVTLL-O	ModPrsL	Module Present
28	LVTLL-O	IntL	Interrupt
29		VccTx	+3.3V Power Supply Transmitter
30		Vcc1	+3.3V Power Supply
31	LVTLL-I	LPMode	Low Power Mode
32		GND	Module Ground

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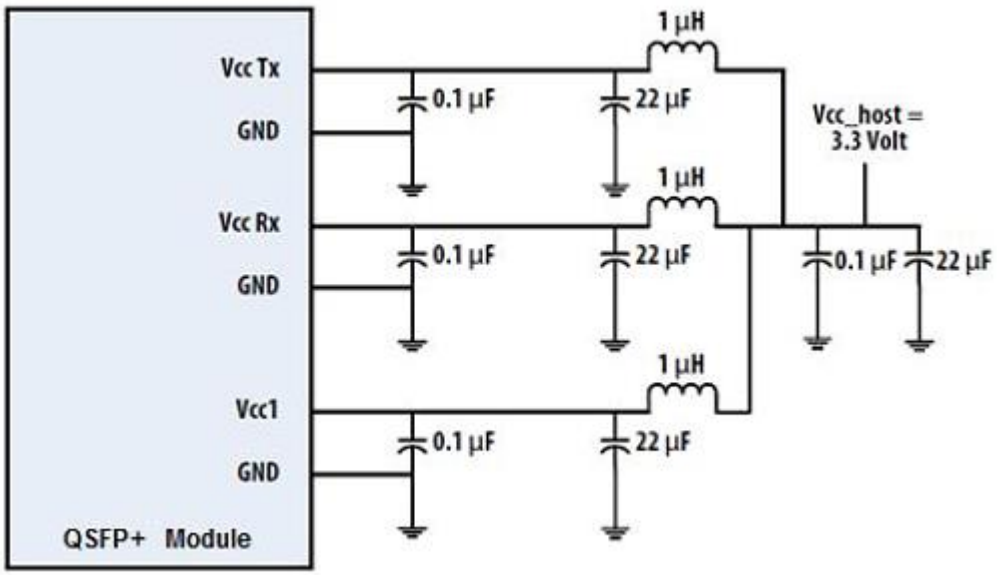
33	CML-I	Tx3p	No Use
34	CML-I	Tx3n	No Use
35		GND	Module Ground
36	CML-I	Tx1p	No Use
37	CML-I	Tx1n	No Use
38		GND	Module Ground

Note1: GND is the symbol for signal and supply (power) common for QSFP28 modules. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground lane.

Note2: VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP28 transceiver module in any combination. The connector pins are each rated for a maximum current of 1000mA.

Recommended Power Supply Filter



Digital Diagnostic Functions

As defined by the QSFP+ MSA, Ficer's QSFP+ transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

- Transceiver temperature
- Laser bias current (4-Channel)
- Transmitted optical power (4-Channel)
- Received optical power (4-Channel)
- Transceiver supply voltage

It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Controller (DDC) inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the QSFP+ transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the QSFP+ transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 000h to the maximum address of the memory.

For more detailed information including memory map definitions, please see the QSFP+ MSA Specification.

Digital Diagnostic Memory Map

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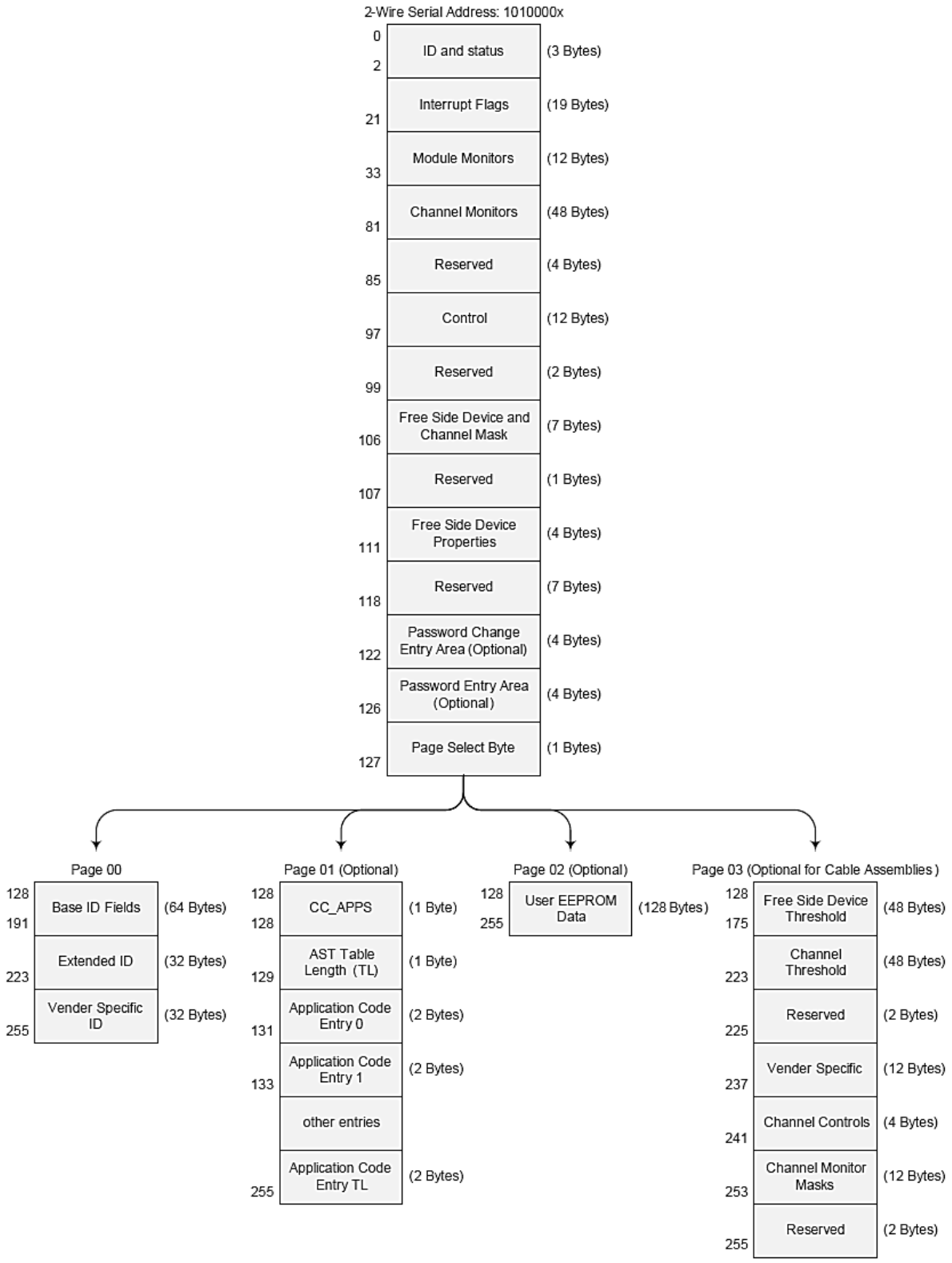
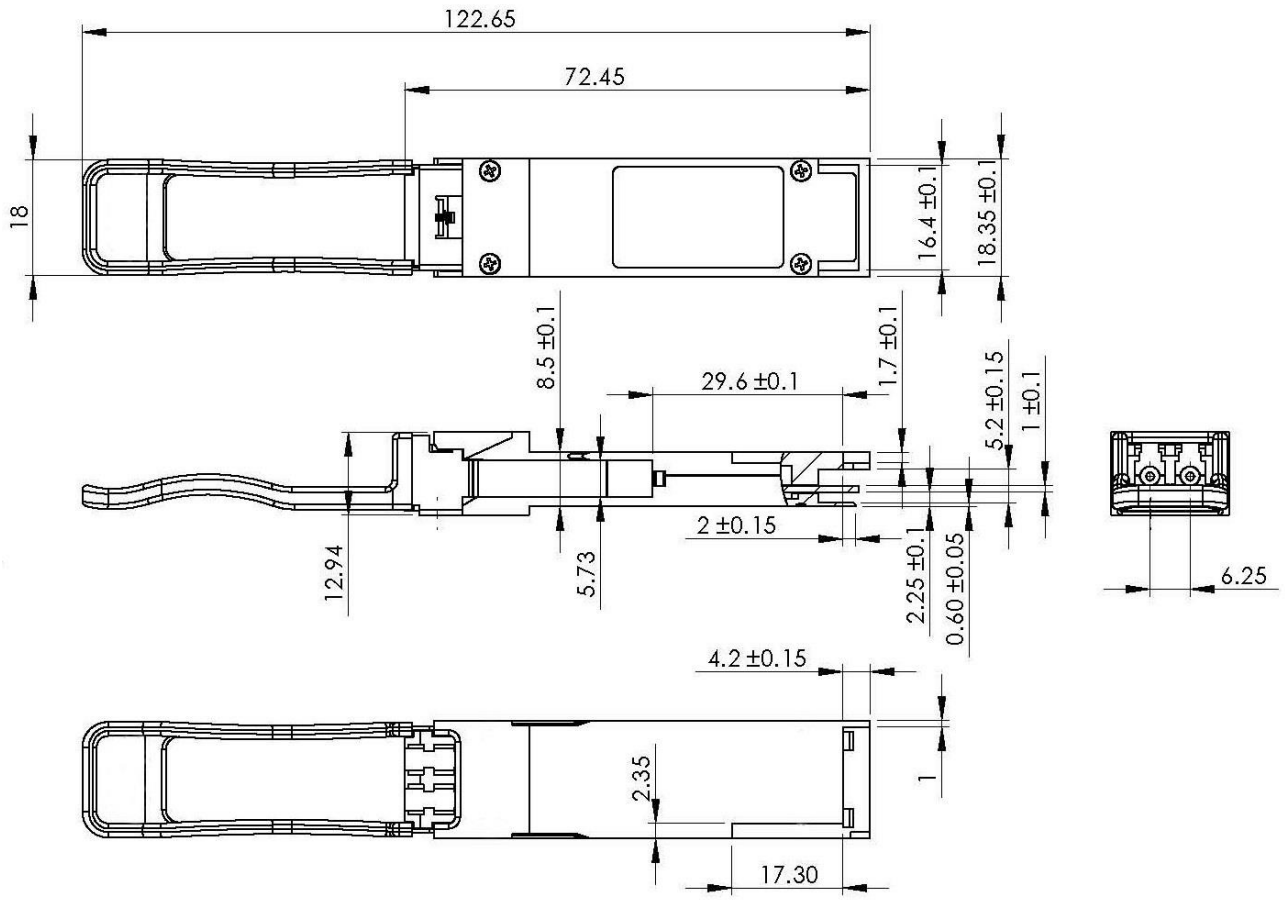

2-Wire Serial Address: 1010000x
0
ID and status
(3 Bytes)
2
Interrupt Flags
(19 Bytes)
21
Module Monitors
(12 Bytes)
33
Channel Monitors
(48 Bytes)
81
Reserved
(4 Bytes)
85
Control
(12 Bytes)
97
Reserved
(2 Bytes)
99
Free Side Device and Channel Mask
(7 Bytes)
106
Reserved
(1 Bytes)
107
Free Side Device Properties
(4 Bytes)
111
Reserved
(7 Bytes)
118
Password Change Entry Area (Optional)
(4 Bytes)
122
Password Entry Area (Optional)
(4 Bytes)
126
Page Select Byte
(1 Bytes)
127
Page 00
128
Base ID Fields
(64 Bytes)
191
Extended ID
(32 Bytes)
223
Vender Specific ID
(32 Bytes)
255
Page 01 (Optional)
128
CC_APPS
(1 Byte)
128
AST Table Length (TL)
(1 Byte)
129
Application Code Entry 0
(2 Bytes)
131
Application Code Entry 1
(2 Bytes)
133
other entries
Application Code Entry TL
(2 Bytes)
255
Page 02 (Optional)
128
User EEPROM Data
(128 Bytes)
255
Page 03 (Optional for Cable Assemblies)
128
Free Side Device Threshold
(48 Bytes)
175
Channel Threshold
(48 Bytes)
223
Reserved
(2 Bytes)
225
Vender Specific
(12 Bytes)
237
Channel Controls
(4 Bytes)
241
Channel Monitor Masks
(12 Bytes)
253
Reserved
(2 Bytes)
255

Mechanical Dimensions



(All Dimensions are ±0.20mm Unless Otherwise Specified, Unit: mm)

Ordering Information

Part No.	Rx	Rx Sensitivity	DDM	Temp.
FQFP-IQ-C85-X1D	908nm 850nm	<-6.5dBm	Yes	0~70°C

Note: Distances are indicative only. To calculate a more precise link budget based on specific conditions in your application, please refer to the optical characteristics.

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